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27660 7590 05/28/2004  
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<b>Bradley J. Berezna</b>	(Depositor's name)
<i>[Signature]</i>	(Signature)
<b>June 22, 2004</b>	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,792	11/25/2003	Donald Ray Disney	03692.P059DC	7244

**TITLE OF INVENTION: METHOD OF FABRICATING A HIGH-VOLTAGE TRANSISTOR WITH A MULTI-LAYERED EXTENDED DRAIN STRUCTURE**

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	08/30/2004

  

EXAMINER	ART UNIT	CLASS-SUBCLASS
NHU, DAVID	2818	438-270000

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**Burgess & Berezna, LLP**  
1  
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(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

**Power Integrations, Inc.**

**San Jose, California**

Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☒ corporation or other private group entity ☐ government

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(Authorized Signature) *[Signature]* (Date) **06/22/04**  
**Bradley J. Berezna**

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**06/28/2004 H0UTEMA2 00000058 10722792**

01 FC:1501	1330.00 OP
02 FC:1504	300.00 OP
03 FC:8001	9.00 OP

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